MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, DOUBLE-EMITTER
TYPES 3N74, TX3N74, 3N75, TX3N75, 3N76, TX3N76, 3N127, TX3N127

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a double-emitter, NPN, silicon tetrode transistor designed primarily for low-power chopper applications. The prefix "TX" is used on devices submitted to and passing the special process-conditioning, testing, and screening specified in 4.5 through 4.5.8.1.

1.2 Physical dimensions. See figure 1 (TO-72).

1.3 Maximum ratings.

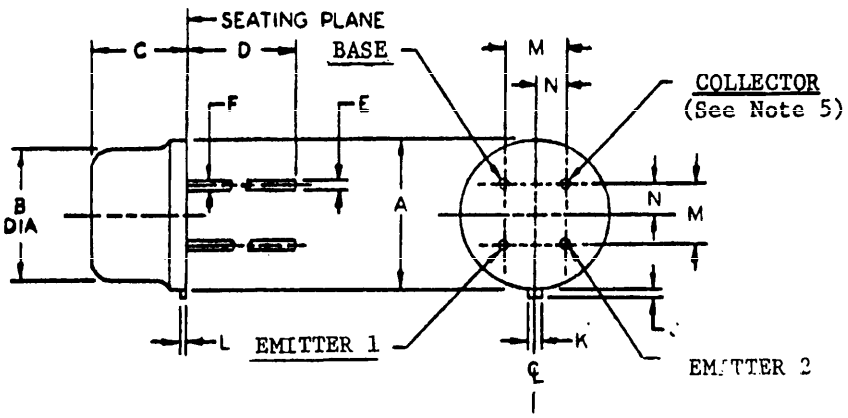
P_T 1/ T_A=25°C		P_T 2/ T_C=25°C		V_{E1E2}	V_{E1B0} or V_{E2B0}	V_{CBO}		I_C	I_B	I_{E_1} or I_{E_2}	T_{stg}
3N74-76	3N127	3N74-76	3N127			3N74-76	3N127				
mW	mW	mW	mW	Vdc	Vdc	Vdc	Vdc	mAdc	mAdc	mAdc	°C
300	200	600	300	20	20	50	30	20	20	10	-65 to +200

1/ Derate linearly 2mW/°C for 3N74-3N76 and 1.33mW/°C for 3N127 for T_A > 25°C.

2/ Derate linearly 4mW/°C for 3N74-3N76 and 2.0mW/°C for 3N127 for T_C > 25°C.

1.4 Primary electrical characteristics.

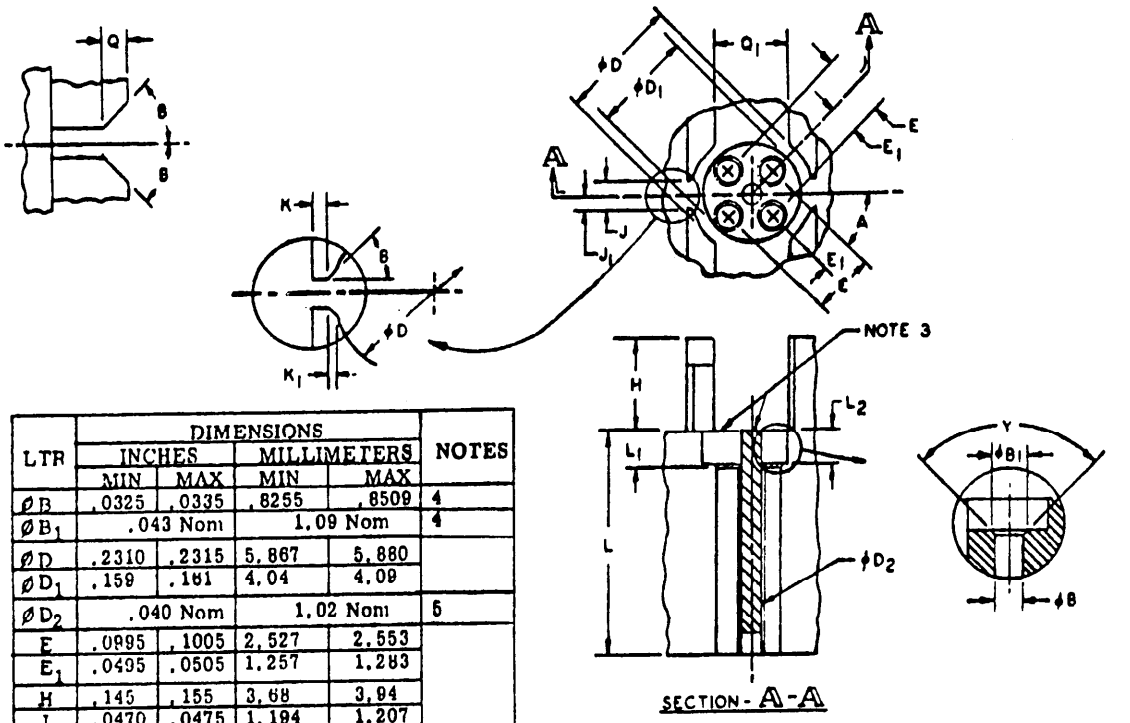
	$\lvert V_{E1E2}(ofs)\rvert$ I_B=-1mAdc I_{E1}=I_{E2}=0 (See figure 3)				$r_{ele2}(on)$ I_B=1mAdc; f=1kHz I_{E1}=I_{E2}=0 (See figure 4)				$\lvert h_{fe}\rvert$ I_C=1mAdc; f=20MHz I_{E1}(or I_{E2})=0				C_{e1b} and C_{e2b} I_C=I_{E1}(or I_{E2})=0 100kHz≤f≤1MHz V_{E1B}(or V_{E2B})=5Vdc	
					I_{e1}=100μAac			I_{e1}=50μAac	V_{CE1}(or V_{CE2})=5Vdc			V_{CE1}(or V_{CE2})=10Vdc		
	3N74	3N75	3N76	3N127	3N74	3N75	3N76	3N127	3N74	3N75	3N76	3N127	3N74-76	3N127
	μVdc	μVdc	μVdc	μVdc	Ω	Ω	Ω	Ω	---	---	---	---	pF	pF
Min	---	---	---	---	10	10	10	1	1.5	1.5	1.5	2.0	---	---
Max	50	100	200	10	40	40	40	25	---	---	---	---	5	2



LTR	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
A	.209	.230	5.31	5.84	
B	.178	.195	4.52	4.95	
C	.170	.210	4.32	5.33	
D	.500	--	12.70	--	7
E	--	.021	--	.53	2,7
F	.016	.019	.41	.48	3,7
J	.028	.048	.71	1.22	6
K	.036	.046	.91	1.17	
L	--	.020	--	.51	
M	.0707 Nom		1.80 Nom		4
N	.0354 Nom		0.90 Nom		4

NOTES:
1. Metric equivalents in table and parentheses are shown for general information only and are based upon 1 inch = 25.4 mm.
2. Measured in the zone beyond .250 (6.35) from the seating plane.
3. Measured in the zone .050 (1.27) and .250 (6.35) from the seating plane.
4. When measured in a gaging plane .054 $^{+.001}_{-.000}$ (1.37 $^{+.03}_{-.00}$) below the seating plane of the transistor, maximum diameter leads shall be within .007 (.18) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance. Figure 2 is preferred measurement method.
5. The collector shall be internally connected to the case.
6. Measured from the maximum diameter of the actual device.
7. All 4 leads.

FIGURE 1. Physical dimensions of transistor types (TX and non-TX) 3N74, 3N75, 3N76, and 3N127 (TO-72).



LTR	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
ØB	.0325	.0335	.8255	.8509	4
$ØB_1$	.043 Nom		1.09 Nom		4
ØD	.2310	.2315	5.867	5.880	
$ØD_1$	.159	.161	4.04	4.09	
$ØD_2$	.040 Nom		1.02 Nom		5
E	.0995	.1005	2.527	2.553	
E_1	.0495	.0505	1.257	1.283	
H	.145	.155	3.68	3.94	
J	.0470	.0475	1.194	1.207	
J_1	.0235	.0245	.597	.622	
K	.009	.011	.229	.279	
K_1	.005 Nom		.127 Nom		
L	.372	.378	9.45	9.60	
L_1	.054	.055	1.37	1.40	
L_2	.043 Nom		1.09 Nom		
Q	.040 Nom		1.02 Nom		
Q_1	.123	.127	3.12	3.23	
A	44.90°	45.10°	--	--	
B	45° Nom		---		
Y	90° Nom		---		

NOTES:
1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. The following gaging procedures shall be used: The device being measured shall be inserted until its seating plane is .125 (3.18 mm) +.010 (.254 mm) from the seating surface of the gage. A force of 8±.5 oz. shall then be applied parallel and symmetrical to the device's cylindrical axis. When examined visually after the force application (the force need not be removed) the seating plane of the device shall be seated against the gage.
   The use of a pin straightener prior to insertion in the gage is permissible.
   A spacer may be used to obtain the .125 (3.18 mm) distance from the gage seat prior to force application.
3. These surfaces to be parallel and in same plane within ±.001 (.025 mm).
4. Four holes.
5. Pressed in.

FIGURE 2. Gage for lead and tab location for transistor types (TX and non-TX) 3N74, 3N75, 3N76, and 3N127.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500—Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-202—Test Methods for Electronic and Electrical Component Parts.
MIL-STD-750—Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 General. Requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500, and as follows:

BV_{E1E2}	Breakdown voltage, emitter one to emitter two, collector short-circuited to base and open circuited to emitters.
C_{e1b} or C_{e2b}	Common base open circuit input capacitance.
I_e	Emitter current (r.m.s.).
I_{E1E2}	Emitter to emitter cutoff current, collector short-circuited to base and open circuited to emitters.
$r_{e1e2}(on)$	Dynamic "on" series impedance between emitter one and emitter two.
V_{E1E2}	Emitter one to emitter two voltage (d.c.).
$\lvert V_{E1E2}(ofs) \rvert$	Magnitude of emitter to emitter offset voltage (d.c.). This term is defined as the open circuit voltage appearing between the two emitters when the collector-base junction is forward biased.
$\lvert \Delta V_{E1E2}(ofs) \rvert_{I_B}$	Magnitude of algebraic difference between offset voltages measured at two different base currents.
$\lvert \Delta V_{E1E2}(ofs) \rvert_{T_A}$	Magnitude of algebraic difference between offset voltages measured at two different temperatures.

3.3 Design and construction and physical dimensions. Transistors shall be of the design, construction, and physical dimensions shown on figure 1.

3.3.1 Lead material and finish. Lead material and finish shall be gold-plated Kovar. (Leads may be tin-coated if specified in the contract or order, and this modification shall not be construed as adversely affecting the Qualified-product Status of the device or applicable JAN marking, see 6.2).

3.4 Performance characteristics. Performance characteristics shall be as specified in tables I and II, and as follows:

3.4.1 Process-conditioning, testing, and screening for "TX" type. Process-conditioning, testing, and screening for the "TX" types shall be as specified in 4.5.

3.5 Marking. The following marking specified in MIL-S-19500 may be omitted from the body of the transistor at the option of the manufacturer:

(a) Country of origin.
(b) Manufacturer's identification.

3.5.1 "TX" marking. Devices in accordance with the "TX" requirements shall include the additional marking "TX" preceding the type designation.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall consist of the examinations and tests specified in tables I and II.

4.2.1 Qualification testing. The non-TX types shall be used for qualification testing. Upon request to the qualifying activity, qualification will be extended to include the "TX" type of the device.

4.3 Quality conformance inspection. Quality conformance inspection shall consist of group A and B inspections. When specified in the contract or order, one copy of the quality conformance inspection data, pertinent to the device inspection lot, shall be supplied with each shipment by the device manufacturer.

4.3.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in table I.

4.3.2 Group B inspection. Group B inpsection shall consist of the examinations and tests specified in table II.

4.4 Methods of examination and test. Methods of examination and test shall be as specified in tables I and II, and as follows:

4.4.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.4.2 Interval for end-point test measurements. End-point tests for qualification and quality conformance inspection shall be completed within 96 hours after completion of the last test in the subgroup.

4.4.3 Emitter to emitter cutoff current. The transistor shall be tested in the circuit shown on figure 5. The specified voltage shall be applied between the two emitter terminals. The current flowing into emitter-one shall then be measured.

4.4.4 Emitter to emitter breakdown voltage. - The transistor shall be tested in the circuit shown on figure 5. The resistor R is a current limiting resistor and should be of sufficiently high resistance to avoid excessive current flowing through the transistor and the current meter. The voltage shall be gradually increased from zero until either the minimum limit of BV_{E1E2} or the specified test current is reached. The transistor is acceptable if the minimum limit for BV_{E1E2} is reached before the test current reaches the specified value. If the specified test current is reached first, the device is rejected.

4.4.5 Emitter to emitter offset voltage. - The transistor shall be tested in the circuit shown on figure 3. The base current shall be adjusted to the specified value. The voltage between the two emitters shall then be measured using a voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement.

4.4.6 Emitter to emitter offset voltage change with base current. - The offset voltage and its polarity shall be measured as specified in 4.4.5 at the two specified base currents. The magnitude of the algebraic difference between these two values shall then be computed.

4.4.7 Emitter to emitter offset voltage change with temperature. - The offset voltage and its polarity shall be measured as specified in 4.4.5 at the two specified temperatures. The magnitude of the algebraic difference between these two values shall then be computed.

4.4.8 Dynamic "on" series impedance. - The transistor shall be tested in the circuit shown on figure 4. The base current shall be adjusted to the specified value and an a.c. sinusoidal signal current of the specified rms value applied through both emitters. The rms voltage, V_{ele2}, between the two emitters shall be measured using an a.c. voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement. The dynamic "on" series impedance shall then be determined as follows:

$$r_{ele2}(on) = \frac{V_{ele2}}{I_{e1}}$$

where V_{ele2} is the rms voltage between the two emitters.

TABLE I. Group A inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	UNIT
Subgroup 1			10	5				
Visual and mechanical examination	2071				---	---	---	---
Subgroup 2			5	2				
Collector to base cutoff current	3036	Bias cond D V_{CB}=30Vdc; I_{E1}=I_{E2}=0			I_{CBO}	---	10	nAdc
Emitter to emitter cutoff current	---	(See 4.4.3)			I_{E1E2}			
3N74,3N75,3N76		V_{CB}=0; V_{E1E2}=+15Vdc				---	+2.0	nAdc
3N127		V_{CB}=0; V_{E1E2}=+10Vdc				---	+0.1	nAdc
Emitter to emitter cutoff current	---	(See 4.4.3)			I_{E1E2}			
3N74,3N75,3N76		V_{CB}=0, V_{E1E2}=-15Vdc				---	-2.0	nAdc
3N127		V_{CB}=0, V_{E1E2}=-10Vdc				---	-0.1	nAdc
Emitter one to base cutoff current	3061	Bias cond D			I_{E1B0}			
3N74,3N75,3N76		V_{E1B}=15Vdc; I_{E2}=I_C=0				---	2.0	nAdc
3N127		V_{E1B}=10Vdc; I_{E2}=I_C=0				---	0.1	nAdc
Emitter two to base cutoff current	3061	Bias cond D			I_{E2B0}			
3N74,3N75,3N76		V_{E2B}=15Vdc; I_{E1}=I_C=0				---	2.0	nAdc
3N127		V_{E2B}=10Vdc, I_{E1}=I_C=0				---	0.1	nAdc
Emitter one to base breakdown voltage	3026	Bias cond D; I_{E1}=10μAdc, I_{E2}=I_C=0			BV_{E1B0}	20	---	Vdc
Emitter two to base breakdown voltage	3026	Bias cond D; I_{E2}=10μAdc, I_{E1}=I_C=0			BV_{E2B0}	20	---	Vdc
Emitter to emitter breakdown voltage	---	I_{E1}=+10μAdc; V_{CB}=0 (See 4.4.4)			BV_{E1E2}	+20	---	Vdc
Emitter to emitter breakdown voltage	---	I_{E1}=-10μAdc; V_{CB}=0 (See 4.4.4)			BV_{E1E2}	-20	---	Vdc

TABLE I. Group A inspection - Continued

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	UNIT
Collector to base breakdown voltage	3001	Bias cond D			BV_{CBO}			
3N74, 3N75, 3N76		I_C=100μAdc; I_{E1}=I_{E2}=0				50	---	Vdc
3N127		I_C=10μAdc; I_{E1}=I_{E2}=0				30	---	Vdc
Subgroup 3			5	3				
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) T_A=25°C I_B=1mAdc; I_{E1}=I_{E2}=0			$\lvert V_{E1E2}(ofs)\rvert$			
3N74						---	50	μVdc
3N75						---	100	μVdc
3N76						---	200	μVdc
3N127						---	10	μVdc
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) I_B=0.2mAdc; I_{E1}=I_{E2}=0			$\lvert V_{E1E2}(ofs)\rvert$			
3N127 only						---	10	μVdc
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) T_A=-25°C I_B=1mAdc; I_{E1}=I_{E2}=0			$\lvert V_{E1E2}(ofs)\rvert$			
3N74						---	50	μVdc
3N75						---	100	μVdc
3N76						---	200	μVdc
3N127							20	uVdc
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) T_A=100°C I_B=1mAdc; I_{E1}=I_{E2}=0			$\lvert V_{E1E2}(ofs)\rvert$			
3N74						---	50	μVdc
3N75						---	100	μVdc
3N76						---	200	μVdc
3N127							20	uVdc
Magnitude of emitter to emitter offset voltage change with temperature	---	(See 4.4.7) I_B=1mAdc; I_{E1}=I_{E2}=0 $T_A(1)$=+100°C			$\lvert \Delta V_{E1E2}(ofs)\rvert_{T_A}$			
3N74		$T_A(2)$=-25°C				---	75	μVdc
3N75		$T_A(2)$=-25°C				---	125	μVdc
3N76		$T_A(2)$=-25°C				---	175	μVdc
3N127		$T_A(2)$=-25°C				---	20	μVdc

TABLE I. Group A inspection - Continued

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN	MAX	UNIT
Magnitude of emitter to emitter offset voltage change with base current	---	(See 4.4.6) $I_B(1)$=1.5mAdc $I_B(2)$=0.5mAdc $I_{E1}=I_{E2}=0$			$\lvert\Delta V_{E1E2}(ofs)\rvert_{I_B}$			
3N74 and 3N75						---	25	µVdc
3N76						---	50	µVdc
3N127							10	uVdc
Subgroup 4			10	5				
Open circuit output capacitance	3236	$I_{E1}=I_{E2}=0$ 100kHz≤f≤1MHz			C_{obo}			
3N74, 3N75, 3N76		V_{CB}=5Vdc				---	8	pF
3N127		V_{CB}=5Vdc				---	4	pF
Common base open circuit input capacitance	3240	$I_C=I_{E2}=0$ 100kHz≤f≤1MHz			C_{e1b}			
3N74, 3N75, 3N76		V_{E1B}=5Vdc				---	5	pF
3N127		V_{E1B}=5Vdc				---	2	pF
Common base open circuit input capacitance	3240	$I_C=I_{E1}=0$ 100kHz≤f≤1MHz			C_{e2b}			
3N74, 3N75, 3N76		V_{E2B}=5Vdc				---	5	pF
3N127		V_{E2B}= 5Vdc				---	2	pF
Magnitude of small-signal short-circuit forward current transfer ratio	3306	I_C=1mAdc; I_{E2}=0 f=20MHz			$\lvert h_{fe1}\rvert$			
3N74, 3N75, 3N76		V_{CE1}=5Vdc				1.5		---
3N127		V_{CE1}=10Vdc				2.0		---
Magnitude of small-signal short-circuit forward current transfer ratio	3306	I_C=1mAdc; I_{E2}=0 f=20MHz			$\lvert h_{fe2}\rvert$			
3N74, 3N75, 3N76		V_{CE2}=5Vdc				1.5		---
3N127		V_{CE2}=10Vdc				2.0		---
Dynamic "on" series impedance	---	(See 4.4.8); f=1KHz I_B=1mAdc; $I_{E1}=I_{E2}=0$			$r_{e1e2}(on)$			
3N74, 3N75		I_{e1}=100µAac rms				10	40	Ω
3N76		I_{e1}=100µAac rms				10	50	Ω
3N127		I_{e1}=50µAac rms				1	50	Ω

TABLE I. Group A inspection - Continued

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX	UNIT
Subgroup 5			10	5				
High temperature operation: Emitter to emitter cutoff current	---	T_A=+100°C (See 4.4.3)			I_{E1E2}			
3N74, 3N75, 3N76		V_{CB}=0; V_{E1E2}=+15Vdc				---	+100	nAdc
3N127		V_{CB}=0; V_{E1E2}=+10Vdc				---	+10	nAdc
Emitter to emitter cutoff current	---	(See 4.4.3) T_A=+100°C			I_{E1E2}			
3N74, 3N75, 3N76		V_{CB}=0; V_{E1E2}=-15Vdc				---	-100	nAdc
3N127		V_{CB}=0; V_{E1E2}=-10Vdc				---	-10	nAdc

TABLE II. Group B inspection

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX	UNIT
Subgroup 1			20	20				
Physical dimensions	2066	(See figure 1)			---	---	---	---
Subgroup 2			15	15				
Solderability	2026				---	---	---	---
Thermal shock (temperature cycling)	1051	Test cond C			---	---	---	---
Thermal shock (glass strain)	1056	Test cond A			---	---	---	---
Seal (leak rate)	---	Method 112 of MIL-STD-202, test cond C, procedure III, test cond A for gross leaks			---	---	$1x10^{-7}$	atm cc/sec

TABLE II. Group B inspection - Continued

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX	UNIT
Moisture resistance	1021				---	---	---	---
End-points:								
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) T_A=25°C I_B=1mAdc; I_{E1}=I_{E2}=0			$\lvert V_{E1E2}(ofs) \rvert$			
3N74						---	50	µVdc
3N75						---	100	µVdc
3N76						---	200	µVdc
3N127						---	10	µVdc
Emitter one to base cutoff current	3061	Bias cond D			I_{E1BO}			
3N74, 3N75, 3N76		V_{E1B}=15Vdc; I_{E2}=I_C=0				---	4	nAdc
3N127		V_{E1B}=10Vdc; I_{E2}=I_C=0				---	0.25	nAdc
Emitter two to base cutoff current	3061	Bias cond D			I_{E2BO}			
3N74, 3N75, 3N76		V_{E2B}=15Vdc; I_{E1}=I_C=0				---	4	nAdc
3N127		V_{E2B}=10Vdc; I_{E1}=I_C=0				---	0.25	nAdc
Subgroup 3			15	15				
Shock	2016	Nonoperating; 1,500G 0.5msec; 5 blows in each orientation X_1, Y_1, Y_2, and Z_1			---	---	---	---
Vibration, variable frequency	2056				---	---	---	---
Constant acceleration	2006	20,000G in each orientation: X_1, Y_1, Y_2, and Z_1			---	---	---	---
End-points:								
(Same as subgroup 2)								

TABLE II. Group B inspection - Continued

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX.	UNIT
Subgroup 4			20	20				
Terminal strength (lead fatigue)	2036	Test cond E			---	---	---	---
Subgroup 5			15	15				
Salt atmosphere (corrosion)	1041				---	---	---	---
End-points:								
(Same as subgroup 2)								
Subgroup 6			λ=10	λ=5				
High-temperature life (nonoperating)	1031	T_{stg}=+200°C			---	---	---	---
End-points:								
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) T_A=25°C I_B=1mAdc; I_{E1}=I_{E2}=0			$\lvert V_{E1E2}(ofs)\rvert$			
3N74						---	75	µVdc
3N75						---	150	µVdc
3N76						---	300	µVdc
3N127						---	15	µVdc
Emitter one to base cutoff current	3061	Bias cond D			I_{E1BO}			
3N74, 3N75, 3N76		V_{E1B}=15Vdc; I_{E2}=I_C=0				---	4	nAdc
3N127		V_{E1B}=10Vdc; I_{E2}=I_C=0				---	0.25	nAdc nAdc
Emitter two to base cutoff current	3061	Bias cond D			I_{E2BO}			
3N74, 3N75, 3N76		V_{E2B}=15Vdc; I_{E1}=I_C=0				---	4	nAdc
3N127		V_{E2B}=10Vdc; I_{E1}=I_C=0				---	0.25	nAdc nAdc

TABLE II. Group B inspection - Continued

EXAMINATION OR TEST	MIL-STD-750		LTPD		SYMBOL	LIMITS		
	METHOD	DETAILS	NON TX	TX		MIN.	MAX	UNIT
Dynamic "on" series impedance	---	(See 4.4.8); f=1kHz I_B=1mAdc; $I_{E1}=I_{E2}$=0			$r_{ele2}(on)$			
3N74, 3N75		I_{e1}=100μAac rms				---	48	Ω
3N76		I_{e1}=100μAac rms				---	60	Ω
3N127		I_{e1}=50μAac rms				---	60	Ω
Subgroup 7			λ=10	λ=5				
Steady state operation life	1026	T_A=25°C; V_{CE}=16Vdc V_{E1E2}=0			---	---	---	---
3N74, 3N75, 3N76		P_T=300mW						
3N127		P_T=200mW						
End points:								
(Same as subgroup 6)								

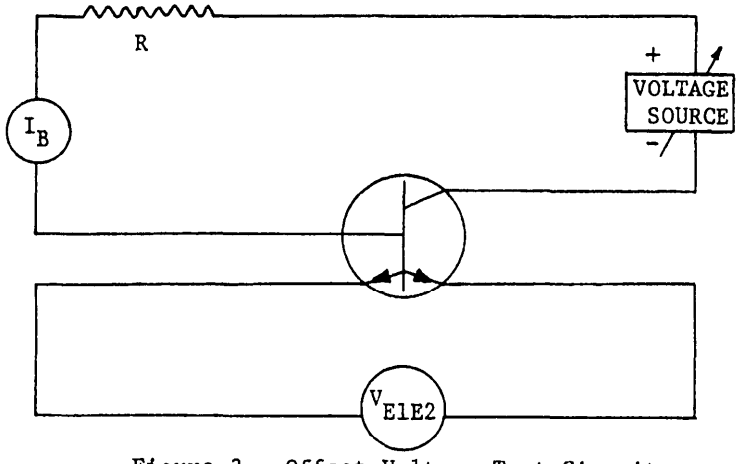


Figure 3. Offset Voltage Test Circuit.

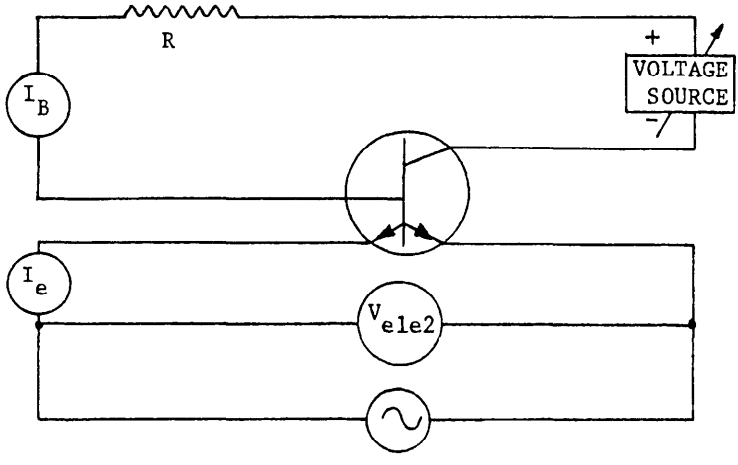


Figure 4. Dynamic "on" series impedance test circuit.

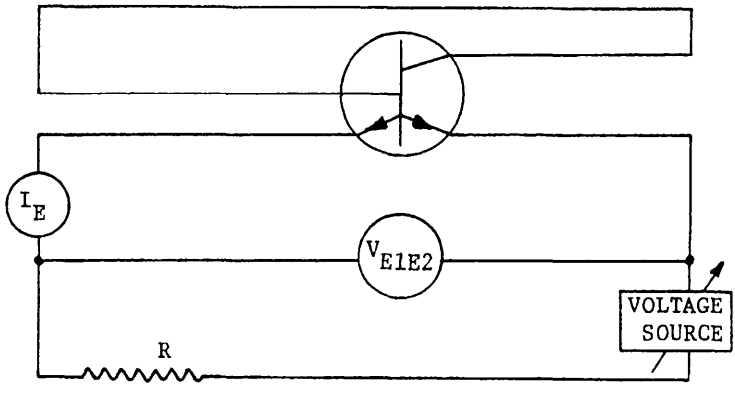


Figure 5. Emitter to emitter cutoff current and emitter to emitter breakdown voltage test circuit.

4.5 Process-conditioning, testing, and screening for TX types. The procedure for process-conditioning, and testing and screening shall be in accordance with 4.5.1 through 4.5.8.1 and figure 6. Process-conditioning shall be conducted on 100 percent of the lot, prior to submission of the lot to the tests specified in tables I and II. (At the option of the manufacturer, the non-TX type may be subjected to process-conditioning and testing.)

4.5.1 Quality assurance (lot verification). Quality assurance shall keep lot records for 3 years minimum, monitor for compliance to the prescribed procedures, and observe that satisfactory manufacturing conditions and records on lots are maintained for these devices. The records shall be available for review by the customer at all times. The quality-assurance monitoring shall include, but not be limited to: process-conditioning, testing, and screening. (The conditioning and screening tests performed as standard production tests need not be repeated when these are predesignated and acceptable to the government as being equal to or more severe than specified herein.)

4.5.2 High-temperature storage. All devices shall be stored for at least 24 hours at a minimum temperature (T_A) of 200°C.

4.5.3 Thermal shock (temperature cycling). All devices shall be subjected to thermal shock (temperature cycling) in accordance with MIL-STD-750, method 1051, test condition C, except that 10 cycles shall be continuously performed and the time at the temperature extremes shall be 15 minutes minimum.

4.5.4 Acceleration. All devices shall be subjected to acceleration test in accordance with MIL-STD-750, method 2006, with the following exceptions: The test shall be performed one time in the Y_1 orientation only, at a peak level of 20,000G minimum. The one minute hold-time requirement shall not apply.

4.5.5 Hermetic seal (fine-leak) test. All devices shall be fine-leak tested in accordance with MIL-STD-202, method 112, test condition C, procedure IIIa or IIIb (using the applicable conditions of 4.5.5.1 or 4.5.5.2), except that the gross leak test shall be as specified in 4.5.5.3.

4.5.5.1 Conditions for procedure IIIa. The devices shall be placed in a sealed chamber and pressurized to 50 psig minimum with the helium gas for a minimum of 4 hours. The devices shall then be removed from the chamber and within 30 minutes be subjected to a helium leak detection test. Devices shall be rejected that exhibit a leak rate of 5×10^{-7} cubic centimeter (cc) of helium per second when measured at a differential pressure of one atmosphere. All devices exhibiting this leakage rate or greater shall be removed from the lot.

4.5.5.2 Conditions for procedure IIIb. The devices shall be placed in an activation tank which shall be pressurized with Krypton 85 tracer gas in a nitrogen solution for sufficient time to detect a leak rate of 1×10^{-8} atmospheric cubic centimeters per second (atm cc/sec). Within four hours after pressurization in the Krypton 85 gas, the leak rate of the devices shall be determined on an attribute basis using the general equation shown below. Any device exhibiting a leak rate equal to or greater than 1×10^{-8} atm cc/sec shall be removed from the lot. The general equation for use with radioactive-gas leak test equipment is:

$$Q = \frac{R}{SKT(P_e^2 - P_i^2)}$$

where:

Q = leak rate in atm cc/sec.
R = net counting rate of tested part above background in cts/min.
S = specific activity of the test gas mixture in μCi/atm cc.
K = counting efficiency of the system for the given part in cts/min μCi.
P_e = pressure of test gas in activation tank during pressurization in atm abs.
P_i = pressure inside part under test in atm abs.
T = duration of pressurization in test gas mixture in seconds.

4.5.5.3 Gross leak test (liquid immersion). All devices shall be tested for gross leaks by immersing in noncorrosive ethylene glycol at approximately 100°C for a minimum of 15 seconds and observed for bubbles. All devices that bubble shall be removed from the lot.

4.5.6 Pre burn-in tests. The parameters $|V_{E1E2}(ofs)|$; I_{E1BO}; I_{E2BO}; and $r_{e1e2}(on)$ of table III shall be measured and the data recorded for all devices in the lot. All devices shall be handled or identified such that the delta end points can be determined after the burn-in test. All devices which fail to meet these requirements shall be removed from the lot and the quantity removed shall be noted on the lot history.

4.5.7 Burn-in test. All devices shall be operated for 168 hours minimum under the following conditions:

T_A = 25°C 3N74, 3N75, 3N76 V_{CE} = 16 Vdc; V_{E1E2} = 0 P_T = 300 mW

3N127 V_{CE} = 16 Vdc; V_{E1E2} = 0 P_T = 200 mW

TABLE III. Burn-in test measurements

EXAMINATION OR TEST	MIL-STD-750		SYMBOL	LIMITS		
	METHOD	DETAILS		MIN	MAX	UNIT
Magnitude of emitter to emitter offset voltage	---	(See 4.4.5) T_A=25°C I_B=1mAdc; I_{E1}=I_{E2}=0	$\|V_{E1E2}(ofs)\|$			
3N74				---	50	µVdc
3N75				---	100	µVdc
3N76				---	200	µVdc
3N127				---	10	µVdc
Emitter one to base cutoff current	3061	Bias cond D	I_{E1BO}			
3N74,3N75,3N76		V_{E1B}=15Vdc; I_{E2}=I_C=0		---	2.0	nAdc
3N127		V_{E1B}=10Vdc; I_{E2}=I_C=0		---	0.1	nAdc
Emitter two to base cutoff current	3061	Bias cond D	I_{E2BO}			
3N74,3N75,3N76		V_{E2B}=15Vdc; I_{E1}=I_C=0		---	2.0	nAdc
3N127		V_{E2B}=10Vdc; I_{E1}=I_C=0		---	0.1	nAdc
Dynamic "on" series impedance	---	(See 4.4.8); f= 1kHz I_B=1mAdc; I_{E1}=I_{E2}=0	$r_{e1e2}(on)$			
3N74,3N75		I_{e_1}=100µAac rms		10	40	Ω
3N76		I_{e_1}=100µAac rms		10	50	Ω
3N127		I_{e_1}=50µAac rms		1.0	50	Ω

4.5.8 Post burn-in tests. The parameters $|V_{E1E2}(ofs)|$; I_{E1BO}; I_{E2BO}; and $r_{e1e2}(on)$ of table III shall be retested after burn-in and the data recorded for all devices in the lot. The parameters $|V_{E1E2}(ofs)|$ (for the 3N74-3N76 only) and $r_{e1e2}(on)$ shall not have changed during the burn-in test from the initial value by more than the specified amount as follows:

$|\Delta V_{E1E2}(ofs)|_{0\text{-}168\ Hours}$ = ±25 percent or 15 µVdc whichever is greater.

$\Delta r_{e1e2}(on)$ = ±25 percent or 5 ohms whichever is greater.

4.5.8.1 Burn-in test failures (screening). All devices that exceed the delta (Δ) limits of 4.5.8 or the limits of table III after burn-in, shall be removed from the inspection lot and the quantity removed shall be noted on the lot history. If the quantity removed after burn-in should exceed 10 percent of the total inspection lot on the burn-in test, then the entire lot shall be unacceptable as TX types.

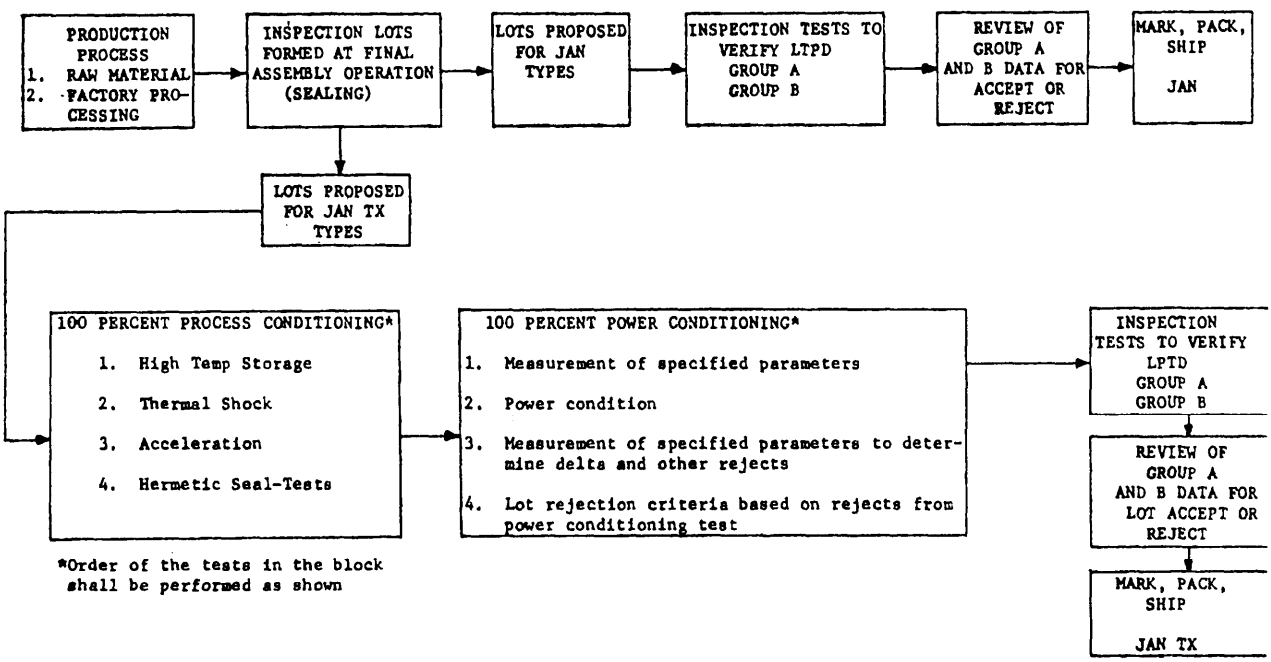


Figure 6. Order of Procedure Diagram for JAN and JAN TX Types

5. PREPARATION FOR DELIVERY

5.1 See MIL-S-19500, section 5.

6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

6.2 Ordering data.

(a) Lead finish if other than gold-plated Kovar. (See 3.3.1.)
(b) Inspection data. (see 4.3.)

6.3 The activity responsible for the Qualified Products List is Rome Air Development Center, Attn: EMTSA, Griffiss Air Force Base, New York 13440; however, information pertaining to the qualification of products may be obtained from the Defense Electronics Supply Center, 1507 Wilmington Pike, Dayton, Ohio 45401.

Custodian:
Air Force - 17

Preparing activity:
Air Force - 17

Review activities:
Air - Force - 11, 85

SPECIFICATION ANALYSIS SHEET

Form Approved
Budget Bureau No. 119-R004

INSTRUCTIONS *This sheet is to be filled out by personnel either Government or contractor, involved in the use of the specification in procurement of products for ultimate use by the Department of Defense. This sheet is provided for obtaining information on the use of this specification which will insure that suitable products can be procured with a minimum amount of delay and at the least cost. Comments and the return of this form will be appreciated. Fold on lines on reverse side, staple in corner, and send to preparing activity (as indicated on reverse hereof).*

SPECIFICATION

ORGANIZATION (Of submitter)	CITY AND STATE
RADC (EMTS)	GRIFFISS AFB, NEW YORK

CONTRACT NO.	QUANTITY OF ITEMS PROCURED	DOLLAR AMOUNT
		$

MATERIAL PROCURED UNDER A

☐ DIRECT GOVERNMENT CONTRACT ☐ SUBCONTRACT

1. HAS ANY PART OF THE SPECIFICATION CREATED PROBLEMS OR REQUIRED INTERPRETATION IN PROCUREMENT USE?

A. GIVE PARAGRAPH NUMBER AND WORDING.

B. RECOMMENDATIONS FOR CORRECTING THE DEFICIENCIES.

2. COMMENTS ON ANY SPECIFICATION REQUIREMENT CONSIDERED TOO RIGID.

3. IS THE SPECIFICATION RESTRICTIVE?

☐ YES ☐ NO IF "YES", IN WHAT WAY?

4. REMARKS *(Attach any pertinent data which may be of use in improving this specification. If there are additional papers, attach to form and place both in an envelope addressed to preparing activity)*

SUBMITTED BY *(Printed or typed name and activity)*	DATE

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